

Liberate

Improve your view...

Liberate is an ultra-fast standard cell and I/O library creator. It generates electrical cell views for timing, power and signal integrity including advanced current source models (CCS and ECSM). It uses a unique “inside view” approach where each cell undergoes a pre-characterization circuit analysis that determines all the necessary stimulus and internal logic states to ensure a complete, accurate and highly efficient characterization of that cell. Liberate supports complex cells including those required for low power design such as state retention flip-flops, level shifters, power switches and MTCMOS cells with sleep modes.

Designing in nanometer process technologies requires many additional library views in order to achieve high quality silicon and avoid silicon re-spins due to inaccurate signoff analysis. To manage leakage power it is common to have low, typical and high threshold cells each with different power and performance characteristics. Furthermore, for accurate modeling of instance specific voltage variation or temperature gradients it is necessary to characterize each library corner at two or three different voltages or temperatures. For the most advanced processes it is becoming common to offer alternative cell libraries that improve yield at the expense of area and performance. Consequently creation and upkeep of all these library views is becoming a major bottleneck in the design flow.

The “Inside View”

Liberate uses a unique “inside view” pre-characterization circuit analysis to perform vector generation and pruning (binning), automatic indices selection as well as optimization

of timing constraint characterization. This results in an order of magnitude speedup over traditional characterization flows, enabling fully automated library creation overnight.

Parallel Characterization

Liberate can fully exploit a large network of multi-core CPUs via intelligent job distribution (with or without a job queue management system) to achieve almost linear speedup per CPU. Each Liberate characterization client is autonomous, greatly reducing network traffic, file I/O and queue requests. Characterization tasks can be performed using Liberate’s internal SPICE simulator or by an external simulators such as Eldo®, Hspice® and Spectre® at any level of granularity from a single arc to a complete cell.

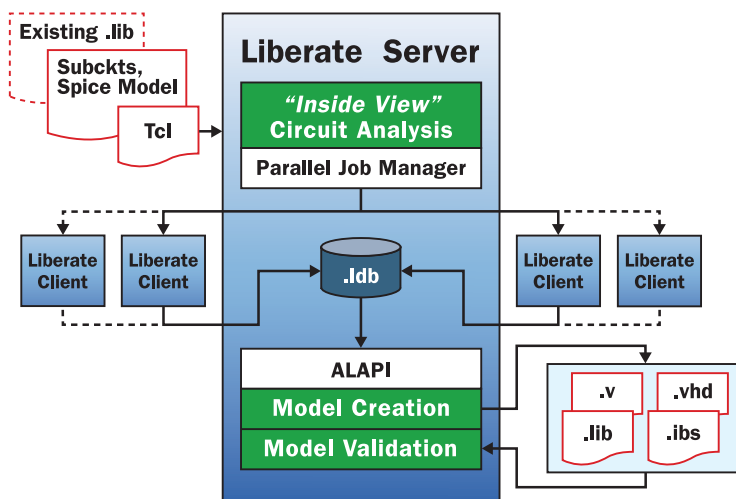
Complex Cell and Model Support

Liberate can characterize highly complex cells including I/Os such as USB and PCIx, clock dividers, pipeline flip-flops, one-hot muxes and custom cells with domino logic. Liberate supports a user specified truth table to drive characterization in addition to automatic vector generation. Complex termination conditions, differential inputs and outputs are also supported as well as simultaneous input switching for creating best-case corners.

Liberate natively generates current source models for both CCS and ECSM, automatically adjusting the waveform segments to minimize the volume of data while ensuring accuracy and consistency with NLDM delay models. For multi-latch cells Liberate automatically determines internal probe points for characterizing timing constraints. For noise view generation, Liberate automatically determines the input and output channel connected logic stages and all the intermediate internal probe points.

Model Generation

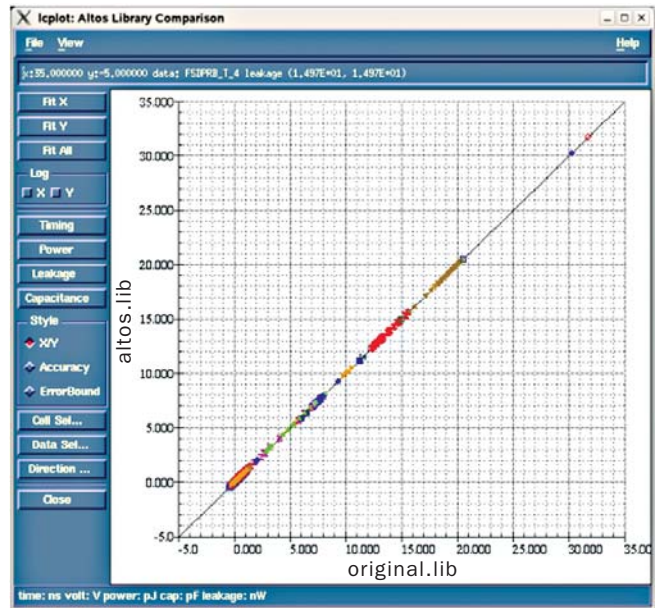
Liberate generates Liberty®, Verilog, Vital and IBIS models, supporting the latest approved format



updates. The models are generated from a central library characterization database (ldb). Multiple versions of library models can be generated from the database to support tools that use older versions of the formats without re-characterization. All the data in the database can be accessed via a Tcl API that can be used to generate proprietary model formats and user specific datasheets by modifying provided examples. The database supports incremental update and can be used to recover from characterization failures caused by network problems.

Model Validation

As the electrical information stored in the library views is used throughout the design process from logic synthesis, through design optimization to final signoff verification, it is essential that the generated libraries are valid and accurate. Liberate includes a number of utilities to verify the generated models including checking for exhaustive state coverage, graphical comparison of library values against a golden reference and verifying the consistency of the logic function derived from the transistor level SPICE sub-circuits against user defined functions (.lib, .v or .vhd formats). In addition, Liberate models have been extensively validated to work with commonly used digital implementation tools from all major vendors including compilation and checking with Library Compiler® and SDF generation and back annotation to Verilog and Vital timing simulation.



Liberate is available on:

- Solaris 9, 10
- RedHat Enterprise Linux 3 update 8 or later, Enterprise Linux 4 update 4 or later
- CentOS 3.8 or later, 4.4 or later

| Feature | Benefit |
|--|--|
| Order of magnitude faster | Faster Time To Market |
| Automatic worst-case vectors | Avoids silicon failures due to incomplete vectors |
| Advanced timing, noise and power models: CCS, ECSM | Better correlation to silicon |
| Low power support | Enables low power design with voltage islands, sleep modes, etc. |

Altos Design Automation
 4020 Moorpark Avenue, Suite 100, San Jose, CA 95117
 Phone 408.980.8056 • Fax 408.557.0637
 Email info@altos-da.com • www.altos-da.com



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