Altos Design Automation

Liberate LV

Improve your view...

Liberate LV provides a collection of utilities for validating libraries including functional equivalence checking, data consistency checking, revision analysis and correlation with various electrical analysis tools for timing (including statistical timing), noise and power. Using Liberate LV a complete validation of a library can be completed overnight on a small number of multi-core computers. For library providers, this assures the library quality before the library is shipped. For library users, it allows cross-checking of the incoming library and provides a clear understanding of the impact of any changes due to newer revisions of cell layouts or process models.

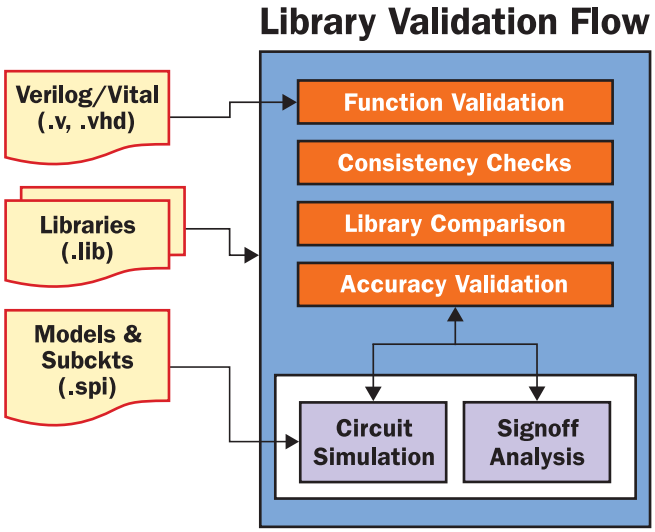
Library characterization requires a complex combination of circuit simulations, data measurements, data collection and formatting, often distributed across a large computer network. In this process there are many opportunities to introduce errors due to network failures, simulation convergence problems, optimistic characterization assumptions, software version incompatibilities, measurement inaccuracy and incorrect user input. Since each library view is used for multiple chip designs, it is paramount that the library data is correct. Liberate LV provides the means to validate and verify the final library to ensure consistency, completeness and accuracy.

Function and State Coverage

To characterize a cell library the input directives, vectors and stimuli often come from a user, provided either as a previous library or hand-coded in the characterization tool's input language. However, these vectors and assumptions may not be consistent with the underlying transistor-level circuits that comprise the current library to be characterized. Liberate LV is able to check all the function descriptions in the input library directly against the transistor-level circuit and report any differences, thus preventing potential functional errors that may occur later when the design is being formally verified or tested after manufacturing.

Liberate LV provides the means to ensure that all the functional information stored in a library (.lib) is consistent between the transistor level SPICE sub-circuits and the library Verilog and/or Vital descriptions.

In addition, Liberate LV will ensure that all the necessary timing, noise, power (both switching and hidden power) and leakage arcs and states are represented in the library and will report any that are missing. Liberate LV will warn where not enough distinct states exist so that potential inaccuracies in downstream tools can be avoided.



Consistency Checks

Liberate LV provides a number of data consistency checks such as comparing table-based nonlinear delay models (NLDM) against current (CCS) and voltage (ECSM) data and checking for non-monotonic delay values.

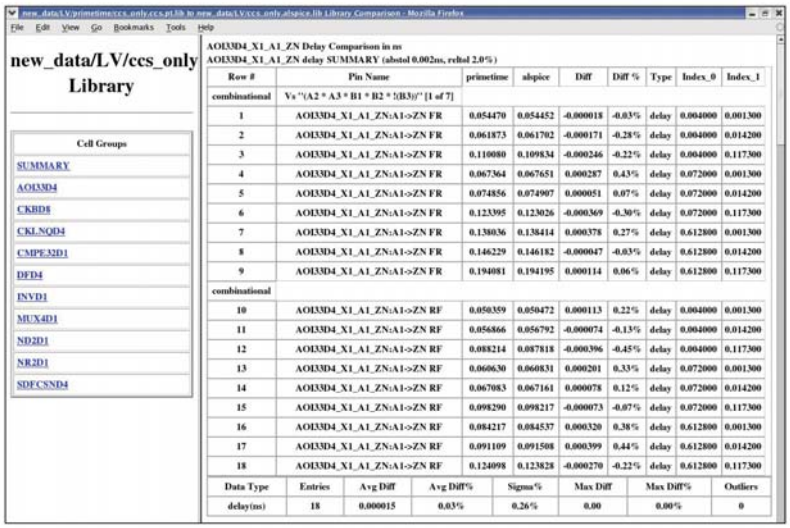
For Verilog and Vital models consistency with the Liberty models (.lib) can be checked by automatically testing SDF back-annotation onto a high level design which instantiates each cell in the library. Multiple SDF generation tools are supported, along with multiple gate level logic simulators such as Mentor Graphics Modelsim®, Synopsys VCS® and Cadence NC-Verilog®.

Library Revisions

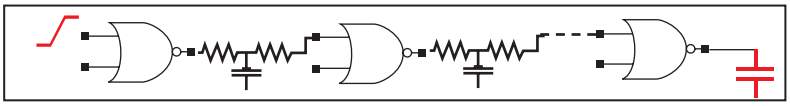
Liberate LV provides the means to compare a new library against an existing golden library, generating both graphical, HTML and text reports. This includes comparing libraries with different indices, different function syntax, different states and even different cell names. This allows verification of libraries created with different characterization systems. It also highlights the impact of each new library revision, detailing changes in delay, capacitance, constraints, switching power, noise and leakage.

Library Validation and Correlation

To verify that the library data is accurate, Liberate LV performs a correlation using the library data in the appropriate analysis tool against results obtained from circuit simulation. To ensure delay accuracy Liberate LV will invoke a static timing analyzer and compare the resulting values against simulation of a test circuit using a SPICE simulator. The test circuits are automatically created, for example as a variable-length chain of cells with interconnect parasitics. Every input-to-output arc will be verified for each logic state, input slew and load condition. Statistical timing analysis tools (SSTA) are also supported by comparing the path mean delay and standard deviation to Monte Carlo Spice simulations.



Liberate LV Timing Validation Comparison Html Report



Liberate LV Sample Test Circuit

Liberate LV also includes the means to measure the accuracy of timing constraints, switching power, leakage and noise. Liberate LV supports multiple analysis tools for timing and noise analysis, e.g. Synopsys PrimeTime SI®, Cadence Encounter® Timing System, Incentia's TimeCraft™ and Extreme DA GoldTime™, as well as numerous SPICE simulators such as Mentor Graphics Eldo™, Synopsys HSPICE® and Cadence Spectre®.

Liberate LV is available on

- Solaris 9, 10
- RedHat Enterprise Linux 3 update 8 or later, Enterprise Linux 4 update 4 or later
- CentOS 3.8 or later, 4.4 or later

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