

# Variety MX

*Improve your view...*

Variety MX expands on Altos' Liberate MX macro block characterization capabilities to include statistical timing models that account for both global (systematic) and local (random) process variation. Variety MX deploys a combination of "dynamic partitioning" and "inside view" transistor analysis techniques to create highly accurate models in typically less than half a day for even million transistor blocks. This is in stark contrast to Monte Carlo analysis which takes weeks for even the smallest macros. The statistical timing models are consistent with Variety's standard cell models and compatible with multiple commercial statistical static timing analyzers.

To accurately model and optimize a chip's performance at advanced process nodes (40nm or below) the contribution of process variation must be accounted for. As variation can come from many sources, some systematic and others random, a statistical static timing approach is most optimal method to accurately predict the true chip performance for both timing closure and manufacturing sign-off. Other methods which assume on-chip process variation causes uniform delay change often lead to over design, impacting design schedule, chip area, power consumption and yield while missing potentially failing paths.

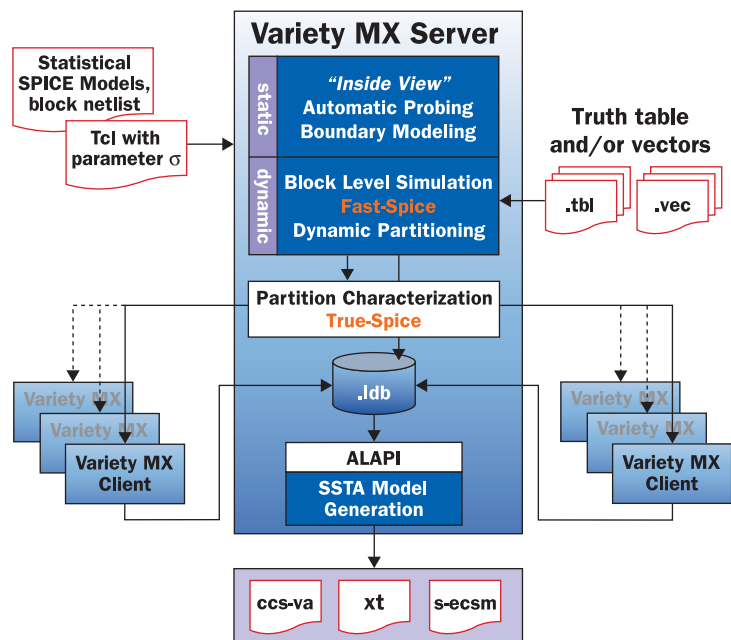
As a large percentage (>50%) of silicon area on most advanced system-on-chip ICs is taken up by large macro blocks such as embedded memory, creation of statistical models for these macros is necessary to perform accurate and complete statistical static timing analysis of the full chip. Using traditional Monte Carlo simulation or even another more optimal sampling simulation technique is not practical for the majority of today's macros that often comprise hundreds of thousands or even millions of transistors. To make statistical block characterization feasible Variety MX combines "dynamic partitioning" with Altos' unique "inside view" pre-characterization transistor analysis.

Dynamic partitioning leverages a single "fast SPICE" simulation run of the complete chip to optimally divide the circuit into critical partitions of typically less than a thousand transistors. Furthermore, the partition size is often independent of the block size especially for regular structures such as embedded memory. As each "dynamic partition" is small enough to be treated as a large cell it can subsequently be characterized using the same proven methods as used by Variety for standard cells.

The "inside view" transistor analysis includes identifying probes to automatically measure timing con-

straints and smart algorithms to improve characterization performance especially for local (random) parameter variation. These include identifying the transistors that are insensitive to a given parameter for each type of arc and hence optimizing the number of simulations necessary to measure the impact of variation while maintaining excellent correlation to Monte Carlo results.

Variety MX creates statistical models for a given set of process parameter variations where the amount of variation is based on statistical SPICE models or actual process measurements. The non-linear sensitivity to process variation for all relevant timing constructs is captured including delay, slew, pin capacitance and timing constraints.



Variety MX							
45nm SRAM Timing Path	Mean Delay SPICE Monte Carlo (ps)	Mean Delay SSTA (ps)	%diff	Delay Sigma SPICE Monte Carlo (ps)	Delay Sigma SSTA (ps)	%diff	Sigma% of Mean
clk->out0	889.2	889.9	0.08%	65.2	66.3	1.69%	7.33%
clk->out1	889.6	889.9	0.03%	66	66.3	0.45%	7.42%
clk->out2	889.2	889.9	0.08%	66.1	66.3	0.30%	7.43%
clk->out3	889.1	889.9	0.09%	65.7	66.3	0.91%	7.39%
clk->out4	888.2	889.9	0.19%	66.2	66.3	0.15%	7.45%
clk->out5	888.4	889.9	0.17%	65.6	66.3	1.07%	7.38%
clk->out6	888.5	889.9	0.16%	66	66.3	0.45%	7.43%

**SPICE Monte Carlo Vs SSTA using models created by Variety MX for a 45nm SRAM**

Variety MX can generate multiple SSTA formats from a single characterization database (ldb). XT format (used by Extreme Design Automation), S-ECSM format (used by Cadence Design Systems) and CCS-VA Liberty variation aware extensions (used by Synopsys) are supported. Custom SSTA formats can be easily added using a Tcl API to the characterization database.

Variety MX supports a number of “fast SPICE” simulators for dynamic partitioning including Synopsys Hsim, Hsim XA and NanoSim, Mentor’s ADiT, Cadence’s Ultrasim and

Infinisim’s OmegaSim. For timing variation characterization Cadence’s Spectre, Synopsys Hspice and Mentor’s Eldo are all supported as well as Altos native Spice engine Alspice.

**Variety MX is available on:**

- RedHat Enterprise Linux 3 update 8 or later
- Enterprise Linux 4 update 4 or later
- CentOS 3.8 or later, 4.4 or later

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